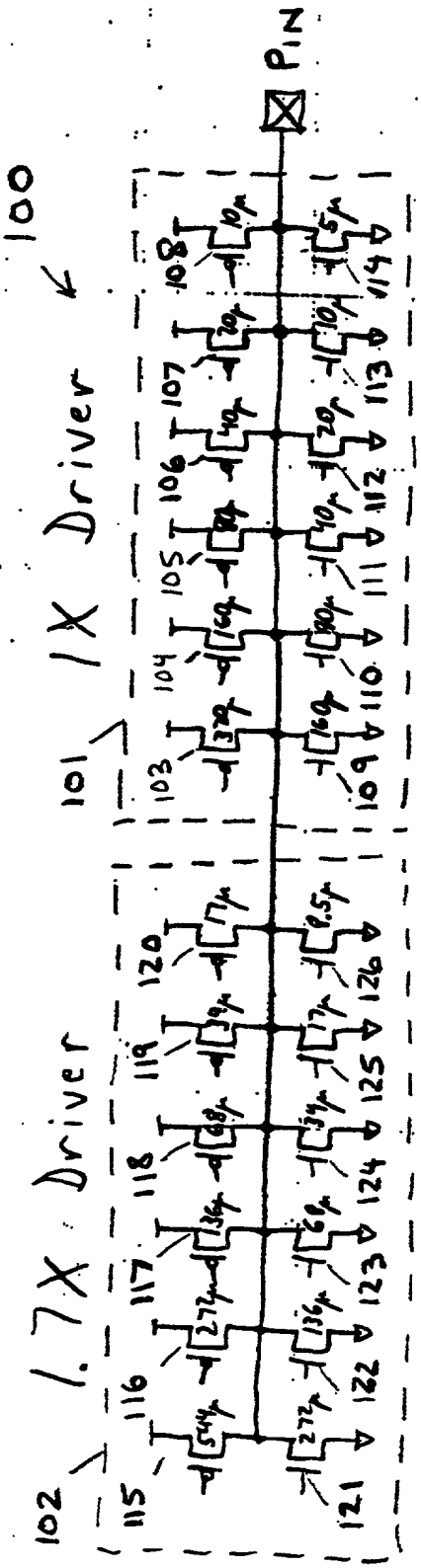


FIG. 1
(PRIOR ART)

20070809.1615.4001

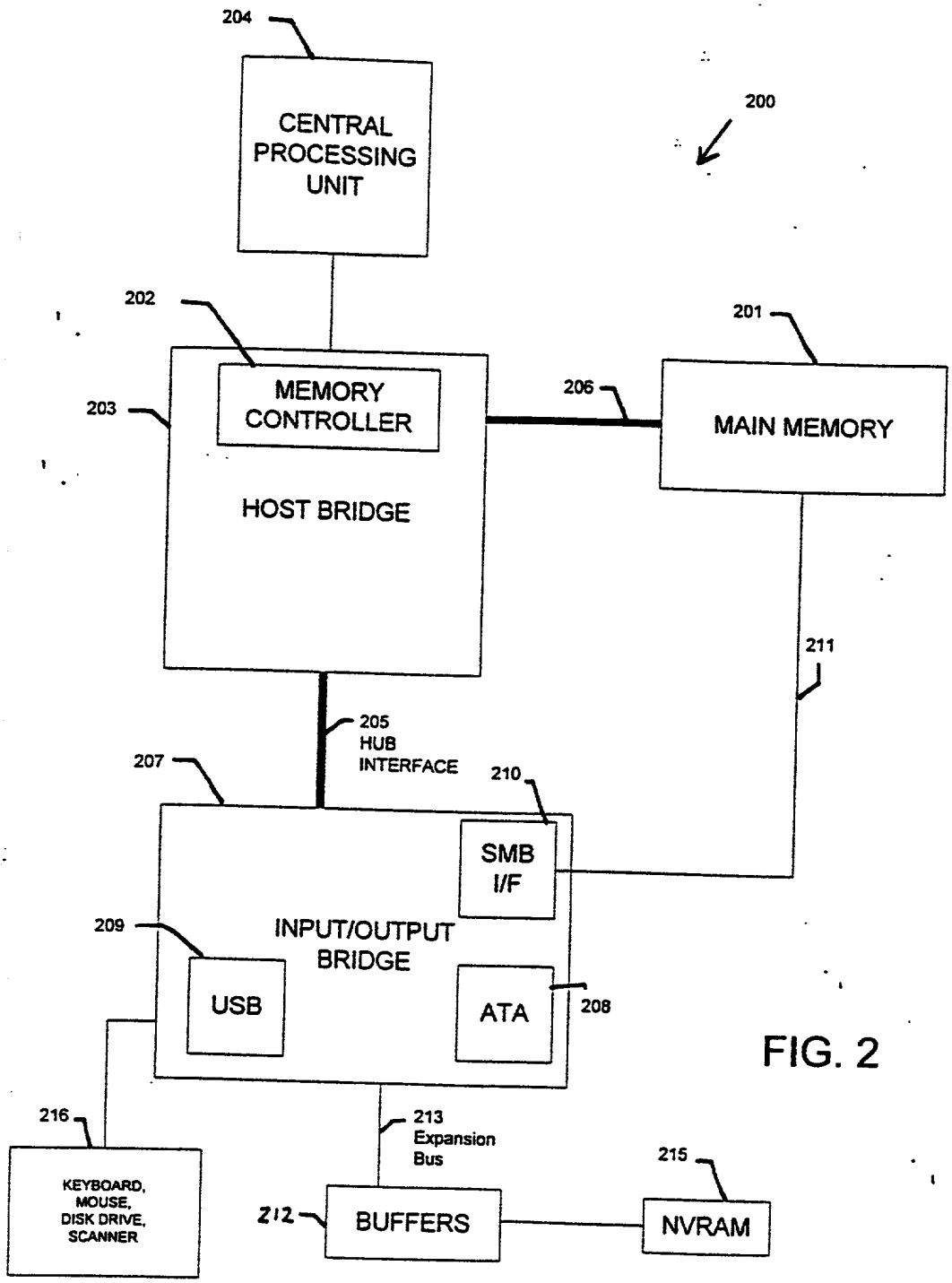


FIG. 2

20030401-0465-1P001

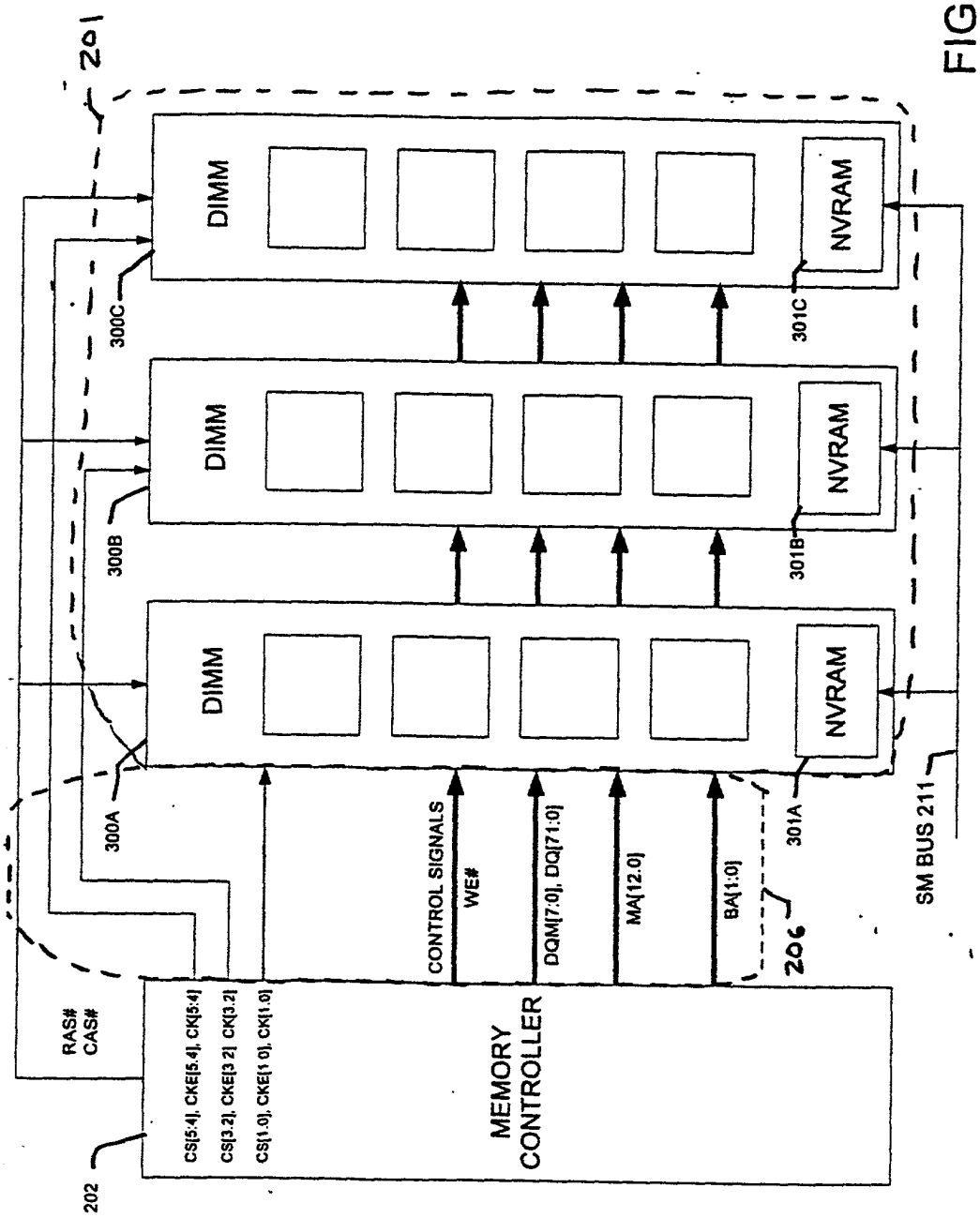
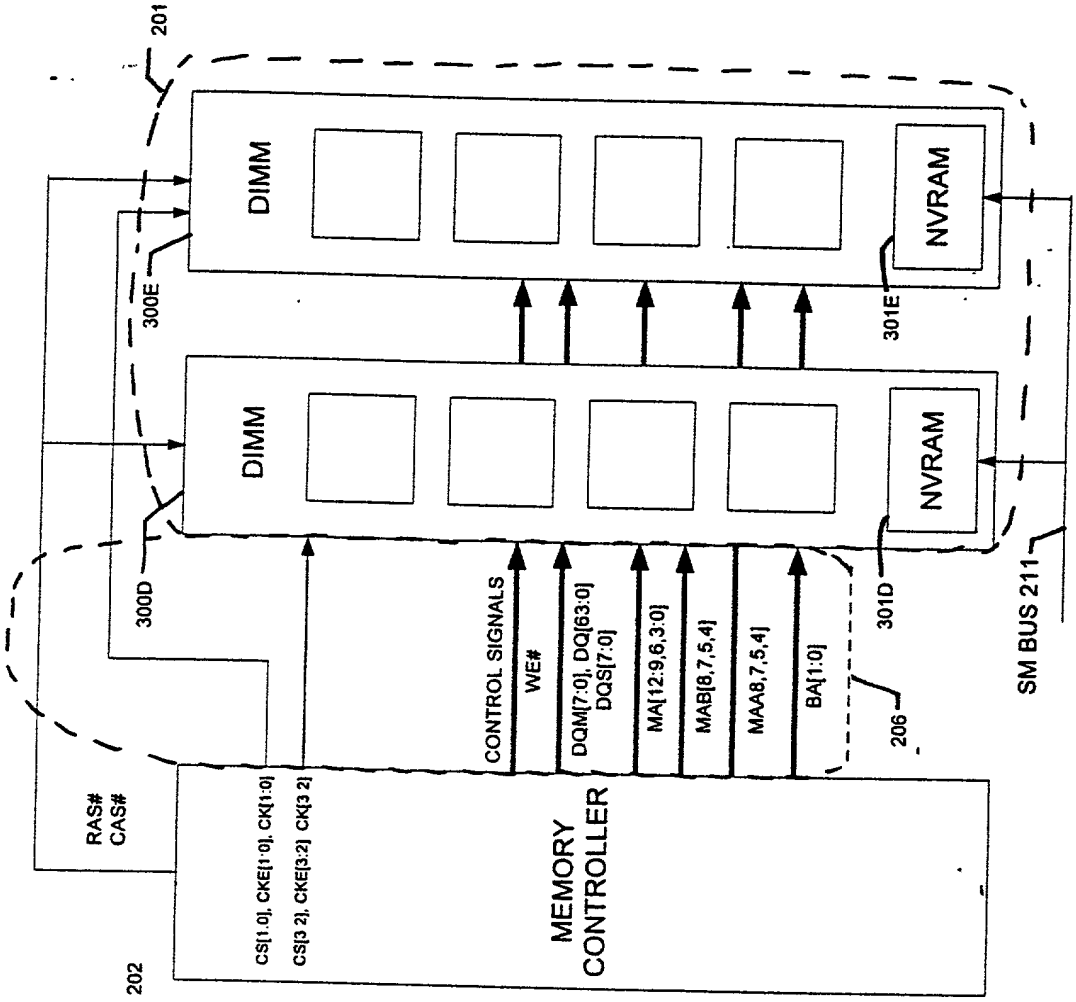

201
DIMM
DIMM
DIMM
NVRAM
NVRAM
NVRAM
300C
300B
300A
301C
301B
301A
SM BUS 211
206
CONTROL SIGNALS
WE#
DQM[7:0], DQ[71:0]
MA[12:0]
BA[1:0]
RAS#
CAS#
CS[5:4], CKE[5:4], CK[5:4]
CS[3:2], CKE[3:2] CK[3:2]
CS[1:0], CKE[1:0], CK[1:0]
MEMORY
CONTROLLER
202

FIG. 3A

FIG. 3B


201
DIMM
DIMM
NVRAM
NVRAM
300E
301E
300D
301D
206
SM BUS 211
CONTROL SIGNALS
WE#
DQM[7:0], DQ[63:0]
DQS[7:0]
MA[12:9,6,3:0]
MAB[8,7,5,4]
MAA8,7,5,4]
BA[1:0]
RAS#
CAS#
CS[1:0], CKE[1:0], CK[1:0]
CS[3:2], CKE[3:2] CK[3:2]
MEMORY
CONTROLLER
202

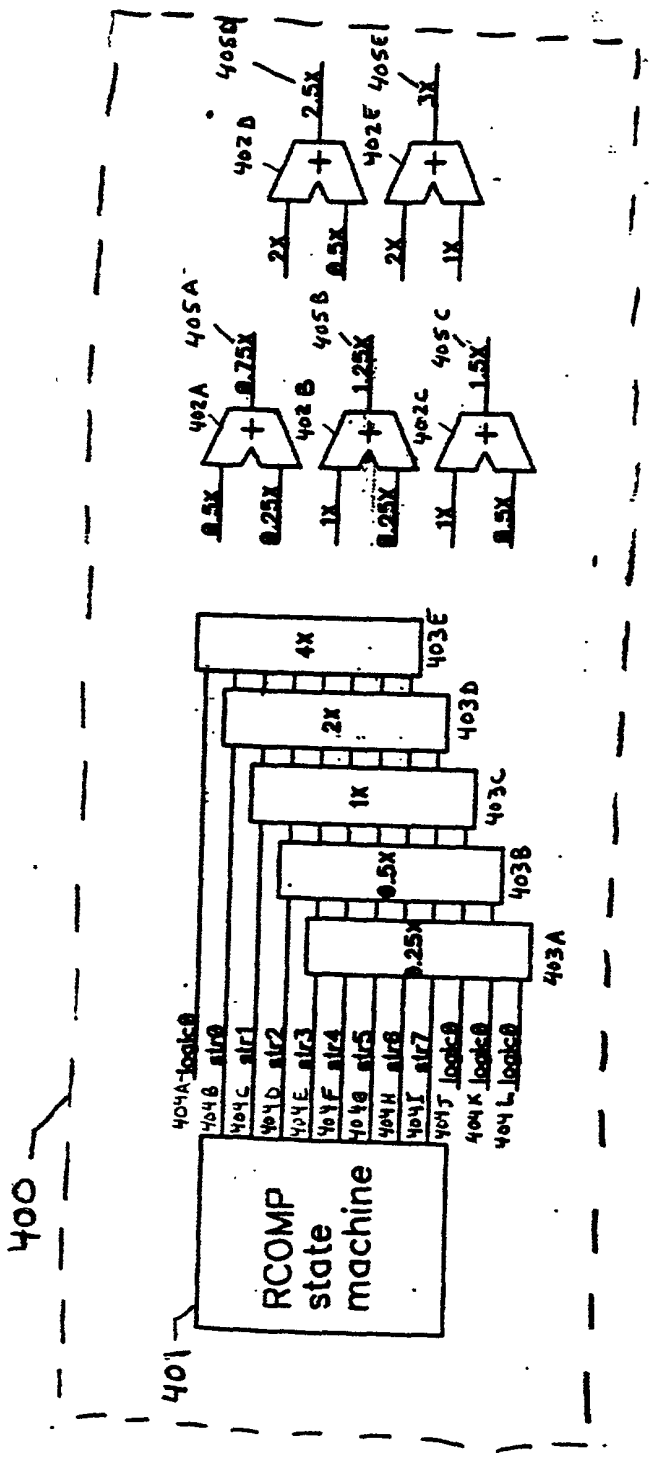

400
401
RCOMP state machine
405A
405B
405C
405D
405E
402A
402B
402C
402D
402E
0.75X
1.25X
1.5X
2.5X
3X
0.5X
0.25X
1X
2X
4X
403A
403B
403C
403D
403E
404A-lock0
404B str0
404C str1
404D str2
404E str3
404F str4
404G str5
404H str6
404I str7
404J lock0
404K lock0
404L lock0

FIG 4

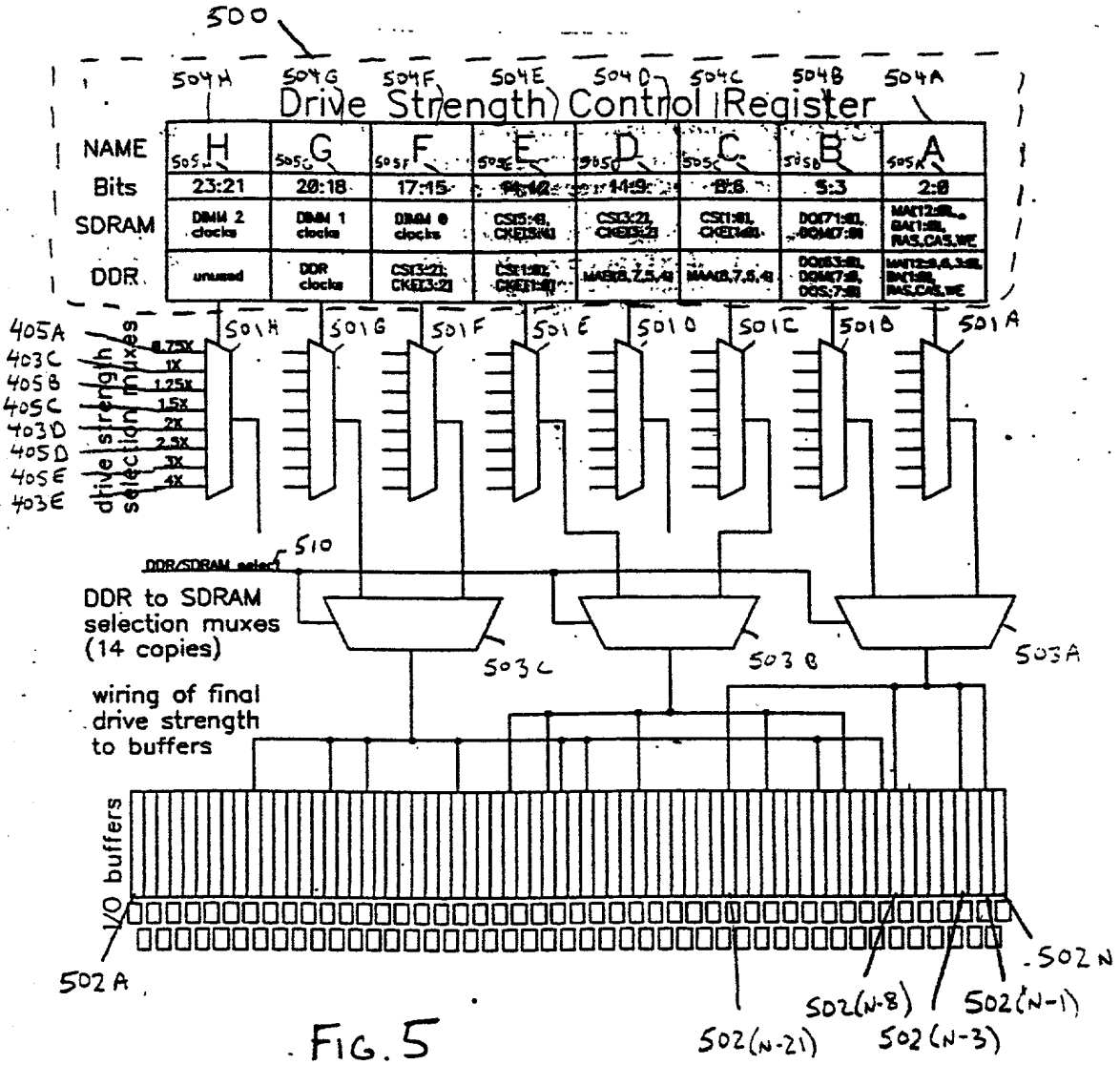

500
504H
504G
504F
504E
504D
504C
504B
504A
Drive Strength Control Register
NAME
Bits
SDRAM
DDR
H
G
F
E
D
C
B
A
23:21
20:18
17:15
14:12
11:9
8:6
5:3
2:0
DIMM 2 clocks
DIMM 1 clocks
DIMM 0 clocks
unused
DDR clocks
501H
501G
501F
501E
501D
501C
501B
501A
405A
403C
405B
405C
403D
405D
405E
403E
drive strength selection muxes
8.75X
1X
1.25X
1.5X
2X
2.5X
3X
4X
510
DDR/SDRAM select
DDR to SDRAM selection muxes (14 copies)
503C
503B
503A
wiring of final drive strength to buffers
I/O buffers
502A
502N
502(N-8)
502(N-1)
502(N-21)
502(N-3)

FIG. 5

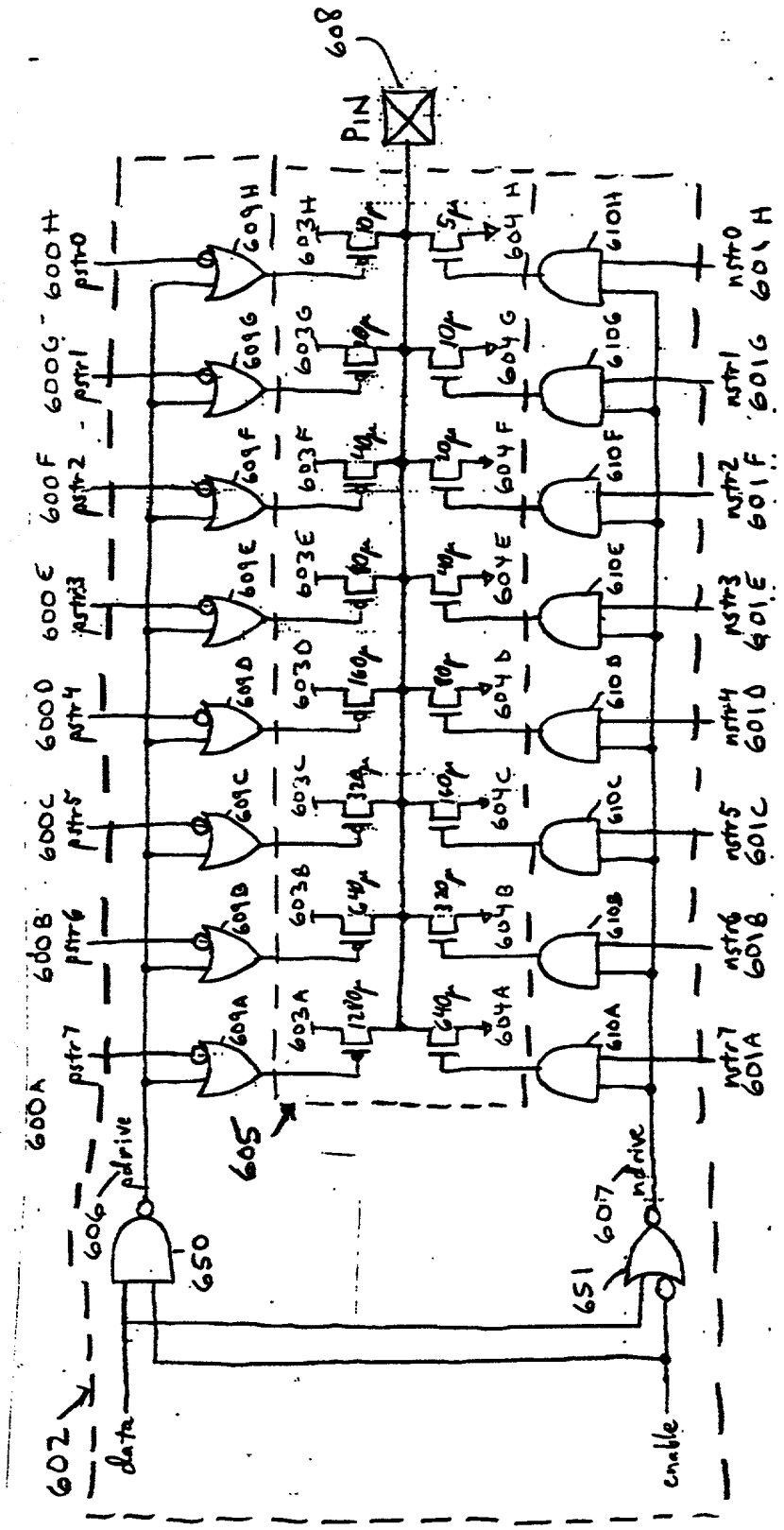

502A
608
PIN
600H
600G
600F
600E
600D
600C
600B
600A
pstr0
pstr1
pstr2
pstr3
pstr4
pstr5
pstr6
pstr7
609H
609G
609F
609E
609D
609C
609B
609A
603H
603G
603F
603E
603D
603C
603B
603A
604H
604G
604F
604E
604D
604C
604B
604A
610H
610G
610F
610E
610D
610C
610B
610A
nstr0
nstr1
nstr2
nstr3
nstr4
nstr5
nstr6
nstr7
601H
601G
601F
601E
601D
601C
601B
601A
605
606
607
650
651
602
data
pdrive
ndrive
enable

FIG. 6